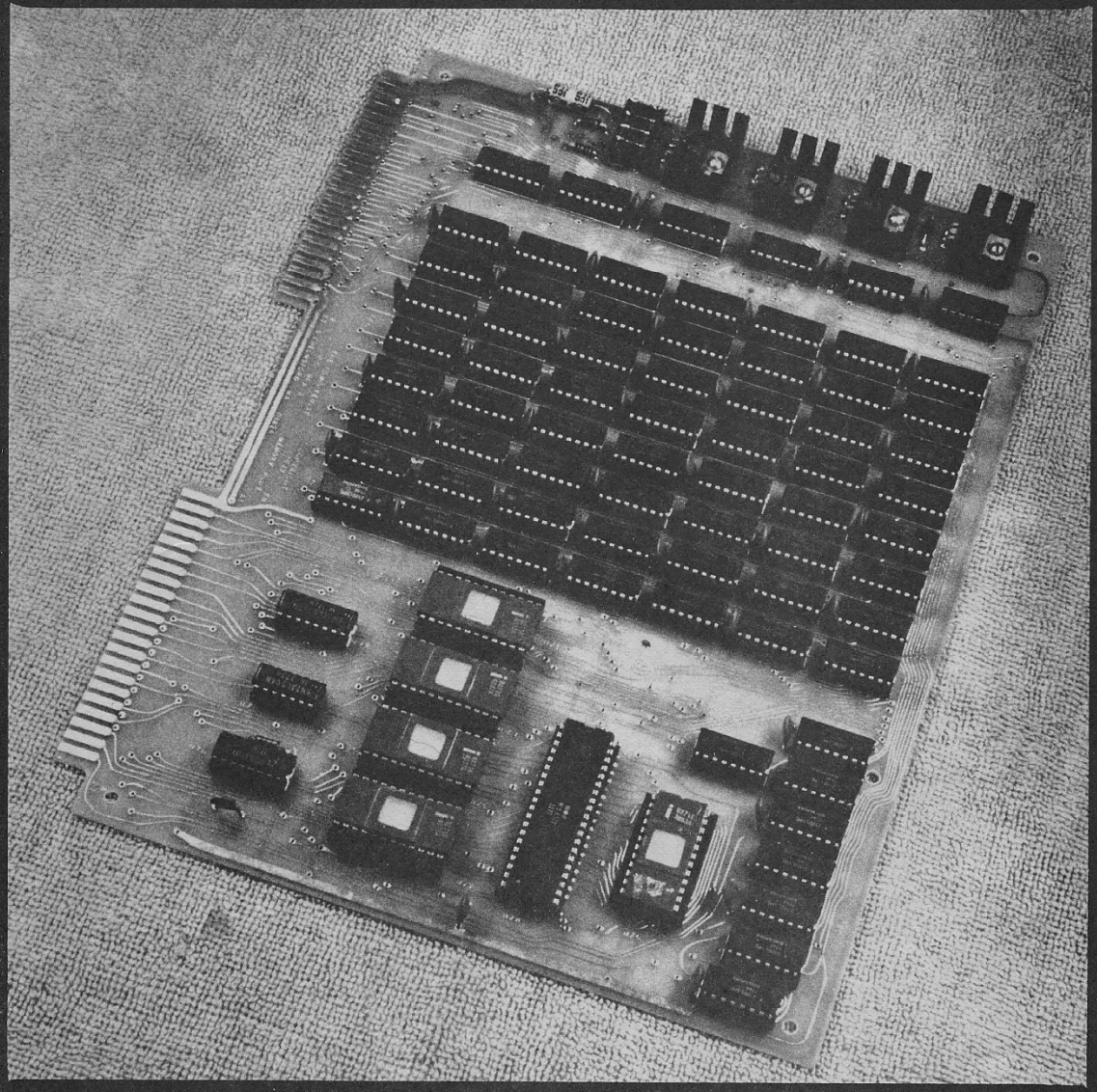
MEMORY PLUS™



FOR THE KIM-1

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MP 2149

Warranty and Service

Should you experience difficulty with your MEMORY PLUS board and be unable to diagnose or correct the problem, you may return the board to The COMPUTERIST for repair. MEMORY PLUS is warranted by The COMPUTERIST against defects in workmanship and materials for a period of ninety (90) days from date of delivery. During the warranty period, The COMPUTERIST will repair or, at its option, replace at no charge components that prove to be defective provided that the board is returned, shipping prepaid, to:

MEMORY PLUS Service Department
The COMPUTERIST, Inc.
56 Central Square
Chelmsford, MA 01824

This warranty does not apply if the board has been damaged by accident or misuse, or as a result of repairs or modification made by other than authorized personnel at the above service facility. No other warranty is expressed or implied. The COMPUTERIST is not liable for consequential damages.

Beyond the ninety (90) day warranty period, MEMORY PLUS boards will be repaired for a reasonable service fee. All service work performed by The COMPUTERIST beyond the warranty period is warranted for an additional ninety (90) day period after shipment of the repaired board.

It is the customer's responsibility to return the board with shipping charges prepaid to the above service facility. For in-warranty service, the board will be returned to the customer, shipping prepaid, by the fastest economical carrier. For out-of-warranty service, the customer will pay for shipping charges both ways. The repaired board will be returned to the customer C.O.D. unless the repairs and shipping charges are prepaid by the customer.

MEMORY PLUS[tm] and Accessories

MEMORY PLUS is a KIM-1 shaped and sized board for extending the capabilities of the KIM-1. It contains 8K RAM (low power 2102 static); provision for up to 8K EPROM (Intel-type 2716 2K by 8-bit); a Versatile Interface Adapter with two 8-bit I/O ports, two timers, and a serial-to-parallel shift register (MOS Technology 6522); and an on board EPROM Programmer. RAM and ROM are each addressable at any 8K (2K hex) boundary and may both be used simultaneously (this is really a 16K board!). Other features are: on board regulators for +5V and +25V, EPROM Programming Program and Memory Test Program on cassette tape, all chips socketted, fully assembled and tested. Connectors, mounting hardware, 60 page manual, etc. included.

Price: $245.00 with everything except the EPROMs.
$40.00 per EPROM
$10.00 for the 60 page Manual (deductable from MEMORY PLUS purchase price).
$10.00 for two Connector Cables ordered with MEMORY PLUS (otherwise $15.00).

POWER PLUS[tm] is a power supply specifically designed for the KIM-1. It has +5V and +12V regulated for the KIM-1 and more than enough +8V unregulated to run the MEMORY PLUS board. It is completely enclosed in a black bakelite case measuring about 6.8" by 5.6" by 3". It is fully assembled and tested. Weight about 3 lbs.

Price: $40.00

ENCLOSURE PLUS[tm] is an enclosure made especially for the KIM-1/MEMORY PLUS combination. It is made of high impact thermoformed plastic and includes a cut-out for the KIM-1 Keypad and a red filter to enhance the visibility of the KIM-1 Display. The MEMORY PLUS board is mounted directly beneath the KIM-1 providing a compact package less than 2.5" high which affords your system a high degree of protection from damage, dust, curious fingers, etc.

Price: $30.00 for complete enclosure.
$10.00 for bottom section only which will permit you to use your existing Enclosure Group SKE 1-1 top section with MEMORY PLUS.

Prices include shipping via U.S. Mail or UPS within the USA. Shipping outside the USA or by other means specified by the purchaser will be billed to the buyer.

Significant discounts are available on quantities of five or more of any item.

Prices and specifications subject to change without notice. The above information is valid as of 1 June 1978. Contact us or your dealer for current pricing info:

The COMPUTERIST, Inc.
P.O. Box 3
S Chelmsford, MA 01824
617/256-3649

Ingenieursbureau koopmans
joh. vermeerstraat 7
papendrecht

Write to the above address for a complete catalog of our products for KIM-1.

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Set Up and Check Out

The quickest way to get your new MEMORY PLUS board "up and running" with your KIM-1 is to take your time and follow all of the steps outlined below.

1. Carefully unpack your MEMORY PLUS board from its individual box, padding, and protective anit-static wrapping. While none of the components on this board are unusally susceptible to static, any chip can be damaged (destroyed) by a large static shock. So, take some care about avoiding static buildup.

2. Examine the board for an visible damage which may have occured in shipping. Push all IC's firmly into their sockets. Unbend any capacitors which have been bent.

3. Read briefly the entire MEMORY PLUS manual. Pay particular attention to the main sections on "POWER", "RAM Memory", "EPROM Memory", and "VERSATILE INTERFACE ADAPTER", but do not try to memorize everything.

4. Build the required connector cables following the wiring list labelled "MEMORY PLUS to KIM-1 Connections". If you are only planning to use the RAM memory to start, then only the expansion connector cable is required, plus a wire running from pin E-16 of MP to A-K of KIM for the DECODE. Remember to remove the wire you currently have between pin A-K of KIM and pin A-1 of KIM which grounds the DECODE signal for an unexpanded system.

5. Carefully check the cable you built for any errors or bad connections.

6. Set up your power for MEMORY PLUS in one of the following ways:

   a. If your have a single +5V supply which is going to run both the KIM-1 and MEMORY PLUS (it must be capable of about 3.5 amps), then the following connections should be made:

      MP E-21 to KIM E-21
      MP E-Y to KIM E-21
      MP A-A to KIM A-A

      The Header should be positioned with the notch at pin 9.

   b. If you have a separate +5V regulated supply for MEMORY PLUS, then the above connections must not be made. The header should be positioned with the notch at pin 9. Attach supply to MP E-21/E-Y.

   c. If you have a +8 to +10 unregulated supply, then the above connections must not be made. The header should be positioned with the notch at pin 1. Attach supply to MP E-19/E-20.

7. Connect the KIM-1 and MEMORY PLUS together via the cables you have made.

8. Set the RAM Select Switch to the 2000 position.

9. Turn on the power supply. Using the KIM-1 monitor, examine and modify a few RAM locations to verify that they basically work. With the RAM switch set to 2000, locations 2000 through 3FFF are accessible. If you are unable to examine and modify these locations, then check steps 2 to 8 for any errors. If you can not find anything you did wrong, then go to the section on "MEMORY PLUS Testing and Field Repair" on page 16.

10. If the above preliminary examination of RAM memory is successful, then you are ready to run a more rigorous memory test. Follow the instructions in the section on "RAM Memory Test". If these tests work, and all you plan to use on MEMORY PLUS is the RAM, then you are done with initial set up and check out.

11. If you plan to use the Versatile Interface Adapter and/or the EPROM Programmer, you must build the cable that goes between the KIM-1 and MEMORY PLUS application connectors if you have not already done so. Follow the wiring list labelled "MEMORY PLUS to KIM-1 Connections". Carefully check the cable you built and review the power connections as discussed in step 6 above.

12. Connect the KIM-1 and MEMORY PLUS together with the application cable.

13. No specific tests are provided for testing the VIA. If you wish to test this chip, read the section on "VERSATILE INTERFACE ADAPTER" and the "MCS6522 VERSATILE INTERFACE ADAPTER - Data Sheet" appendix. You may then devise your own tests dependent on how you intend to use the VIA chip.

14. The only simple way to test the EPROM Programmer is to program an EPROM. The EPROM Programmer requires a +25 volts at 30 milliamps. The best way to provide this is by using the on board regulator circuit. A +27 to +30V unregulated supply can be connected to pin E-3 of the MEMORY PLUS expansion connector. See the section on "EPROM Programming" for details. This will provide about +24.7V for EPROM programming and will prevent over voltages which can destroy an EPROM. Follow the instructions in the "EPROM Programming" section and program an EPROM.

15. Once you have a programmed EPROM, you can place it into the correct EPROM socket and try to use it. The "standard" addresses for the MEMORY PLUS board are C000 - C7FF, C800 - CFFF, D000 - D7FF, and D800 - DFFF. Set the ROM Select Switch to the desired 8K starting address. Since the EPROM Programmer Program verified as it programmed, the contents should be correct. If not, then there is probably a problem in where you have placed the EPROM (wrong socket) or which direction you have inserted the EPROM (pin 1 goes upper right corner). If the contents of the EPROM look okay, then execute the code to determine if it runs correctly. If the code looks correct, then it should run properly.

16. You may now wish to mount the working MEMORY PLUS board under the KIM-1. Use the mounting bolts, nuts, stand-offs and rubber feet provided.

17. Congratulations. You now have an expanded KIM-1 system with a lot of new capabilities. You should now make yourself more familiar with the MEMORY PLUS facilities by re-reading the documentation, particularly the VIA Data Sheet.

MEMORY PLUS to KIM-1 Connections

Function	MEMORY PLUS Pin#	KIM-1 Pin#	Expansion Connector Function	MEMORY PLUS Pin#	KIM-1 Pin#
Ground	E-1	E-22	Ground	E-A	E-22
+5V Battery	E-2		AB0	E-B	E-A
+27 Unreg.	E-3		AB1	E-C	E-B
$\overline{IRQ}$	E-4	E-4	AB2	E-D	E-C
	E-5		AB3	E-E	E-D
	E-6		AB4	E-F	E-E
$\overline{RST}$	E-7	E-7	AB5	E-H	E-F
DB7	E-8	E-8	AB6	E-J	E-H
DB6	E-9	E-9	AB7	E-K	E-J
DB5	E-10	E-10	AB8	E-L	E-K
DB4	E-11	E-11	AB9	E-M	E-L
DB3	E-12	E-12	AB10	E-N	E-M
DB2	E-13	E-13	AB11	E-P	E-N
DB1	E-14	E-14	AB12	E-R	E-P
DB0	E-15	E-15 *	AB13	E-S	E-R
DECODE	E-16	A-K *	AB14	E-T	E-S
	E-17		AB15	E-U	E-T
	E-18		Phase 2	E-V	E-U
+8V Unreg.	E-19		Read/Write	E-W	E-V
+8V Unreg.	E-20		$\overline{Phase\ 2}$	E-X	E-Y
+5V Regulated	E-21	E-21	+5V Regulated	E-Y	E-21
Ground	E-22	E-22	Ground	E-Z	E-22

Function	MEMORY PLUS Pin#	KIM-1 Pin#	Application Connector Function	MEMORY PLUS Pin#	KIM-1 Pin#
Ground	A-1	A-1	+5V Regulated	A-A	A-A
MPA1	A-2		MPB6	A-B	
MPA2	A-3			A-C	
MPA3	A-4			A-D	
MPA4	A-5		MCA1	A-E	
MPA5	A-6		MCA2	A-F	
MPA6	A-7		MCB1	A-H	
MPA7	A-8		MCB2	A-J	
MPB0	A-9		DECODE	A-K	A-K *
MPB1	A-10		K5	A-L	A-H
MPB2	A-11			A-M	
MPB3	A-12			A-N	
MPB4	A-13			A-P	
MPA0	A-14			A-R	
MPB7	A-15			A-S	
MPB5	A-16			A-T	
	A-17			A-U	
$\overline{MCB2}$	A-18			A-V	
PRA8	A-19	A-9		A-W	
PRA9	A-20	A-10		A-X	
PRA10	A-21	A-11		A-Y	
+25V Regulated	A-22			A-Z	

* One of the two DECODE lines must be connected to the KIM-1.

POWER

The power requirements for MEMORY PLUS are simple and on-board regulators are provided to make powering the board even easier. Essentially the board requires only +5 volts at about 2.0 amps. While the actual current requirements will vary slightly with the particular components on any board, the table below shows the individual and collective power requirements.

Component	#	Typical	Maximum	Measured	Max Total	Meas. Total
74LS00	1		8	3	8	3
74LS04	1		8	4	8	4
74LS32	1	5	10	2	10	2
74LS138	3	7	10	6	30	18
74LS367	3	14	24	17	72	51
2716	4	57	105	45	420	180
6522	1	50	[A] 60	52	60	52
2102L [B]	32	14	22	14	704	448
2102L	32	14	22	14	704	448
Total System					2016	1206 [C]

Notes: All current values in milliamps.
[A] Value as estimated by an engineer at MOS Technology.
[B] 2102Ls are split into two sections of 4K RAM each in the table for purposes of discussion below.
[C] Measurements were taken with an inexpensive meter and should be only used as a guide to the system current requirements.
[D] The above values were obtained with Fairchild 21L02s. The values may vary with other 21L02s produced by other manufacturers and supplied with your MEMORY PLUS board.

Regulated +5 Volt Supply. If the MEMORY PLUS is to be powered by regulated +5 volts, then the supply should be connected to pins E-21 and E-Y on the MEMORY PLUS expansion connector. The supply should be capable of supplying at least 2.0 amps in addition to any other board it is driving such as the [illegible]-1. The Header at the top of the board should be positioned so that the bus wires are away from the top of the board and the Header notched corner is positioned at pin 9.

Unregulated +8 to +10 Volt Supply. If the MEMORY PLUS is to be powered by unregulated +8 to +10 volts, then the supply should be connected to pins E-19 and E-20 on the MEMORY PLUS expansion connector. The supply should be capable of supplying at least 2.5 amps. This supply is distributed to three +5 volt regulators which each handle a separate section of the board.

Regulator Q4 supplies the high 4K of 2102L RAM with 448 to 704 milliamps.
Regulator Q5 supplies all support chips, the 2716s and the 6522 with 310 to 608 milliamps.
Regulator Q6 supplies the low 4K of 2102L RAM with 448 to 704 milliamps.

The Header at the top of the board should be positioned so that the bus wires are near the top of the board and the Header notched corner is positioned a pin 1.

The only other power requirement for the MEMORY PLUS board is +25 volts at 30 milliamps during programming of an EPROM. This voltage may be provided as either regulated +25 volt or unregulated +28 to +30 volts.

Regulated +25 Volt Supply. Programming of the INTEL 2716 EPROM requires +25V. This may be attached to pin A-22 of the MEMORY PLUS application connector. Care must be taken to assure that the voltage is within the limits of +24 to +26 volts. A higher voltage will destroy the EPROM as both the INTEL documentation and my own personal experience can attest.

Unregulated +27 to +30 Volt Supply. MEMORY PLUS provides a circuit with a +24 volt regulator and a diode to produce a regulated +24.7 volts from an unregulated +27 to +30 volt supply. The unregulated supply, which may be three +9 volt transistor radio type batteries, is attached to pin E-3 of the MEMORY PLUS expansion connector. Since the programming voltage is so critical and since an over voltage can destroy an EPROM, use of this on board regulator is recommended. The three battery clips provided in the Accessory Bag are for the purpose of hooking up three +9 volt batteries.

Battery Backup. Since it is often desirable to be able to protect the contents of the RAM memory during a transient power interruption, or for longer periods of time, a provision has been made for battery backup to be connected to the MEMORY PLUS board. The batteries must be capable of providing between about 3.5 and 4.5 volts. They are connected to pin E-2 of the MEMORY PLUS expansion connector. There are diodes in the circuit which prevent current from being drawn from the batteries during normal system functioning. When the power drops, however, the batteries will automatically start supplying the required current. The amount of current will depend on the basic system configuration. If the MEMORY PLUS board is being run from +5 volts, then the batteries must supply the entire board. If the board is being run from the +8 to +10 volt regulators, then the battery backup will only run the RAM memory chips. This will result in a lower current drain on the batteries. The length of time that the system will retain its RAM contents on battery power will be a function of the configuration and the capacity of the batteries.

Cassette Loading Instructions

The user is assumed to know the basics of loading cassette tape into a KIM-1. If you are not certain of the procedures, see pages 12 through 16 of the KIM-1 User Manual.

The MEMORY TEST is the first program on the tape. It has Program ID = 10. It loads into locations 0000 through 0092. It is set up to test memory from 2000 to 3FFF. The starting address of the program is 0003. See pages 20 and 21 of this manual for the MEMORY TEST Source Listing and page 19 for instructions on using the program.

The PROM PROGRAMMER is the second program on the tape. It has Program ID = 20. It loads into locations 0000 through 0098. The programming parameters must be set up in locations 0000 through 0005 as outlined in the section on EPROM Programming, pages 11 to 13. The starting address of the program is 0006.

RAM Memory

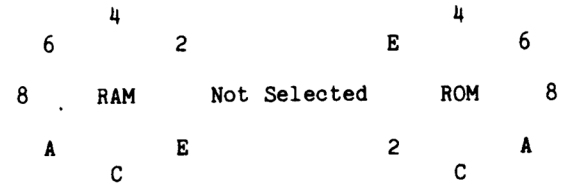
The Random Access Memory (RAM) used with MEMORY PLUS is 2102-type static RAM. This is the same type of RAM used for the main memory on the KIM-1, and is the type of memory that was used in the KIM-2 and KIM-3 memory boards which were offered by MOS Technology. Each 2102 chip contains 1024 bits of memory. Any single bit is directly addressable. By addressing eight chips in parallel, an eight bit word is accessed. It takes eight 2102 chips to provide 1024 8-bit bytes. The MEMORY PLUS provides 8K bytes of 8-bit RAM (actually 8192 bytes). This requires 64 2102 chips: eight chips per 1K times eight K.

The 2102 chips used with MEMORY PLUS are Synertek 21L02B or equivalent. This version of 2102 has the following basic parameters:

SPEED: 450 nanosecond access time
POWER: 30 milliamp worst case (these are "low power" chips)
single +5 voltage required

The MEMORY PLUS RAM is organized into a single contiguous 8K block of memory. The location of the RAM in the KIM-1 addressing space is defined by a switch which may be set to start at any 8K boundary (2K hex boundary). Looking at board with the regulators at the top, The RAM select switch is the left switch of the pair of rotary switches. Using the flat side of the switch as the position indicator, the addresses are set as follows:

On-board Address Select Switches for RAM and ROM



The address associated with each position is:

2K	2000 to 3FFF	Assumed as the RAM address in this manual.
4K	4000 to 5FFF	
6K	6000 to 7FFF	
8K	8000 to 9FFF	
AK	A000 to BFFF	
CK	C000 to DFFF	Assumed as the ROM address in this manual.
EK	E000 to FFFF	Not normally used for RAM since interrupt vectors must be defined in FFFA to FFFF if this memory is addressed. See note in EPROM Memory about using this space for EPROM.

The exact layout of the individual RAM chips may be found in a diagram in the section on "MEMORY PLUS Testing and Field Repair".

EPROM Memory

The Erasable Programmable Read-Only Memory (EPROM) used with MEMORY PLUS is an ultraviolet erasable and electrically programmable 2716 type ROM. This is a fairly new memory chip. The version used in MEMORY PLUS is made by INTEL. It is not compatible with the 2716 made by some other manufacturers such as Texas Instruments. It may be second sourced by other manufacturers, but be certain that any EPROM you purchase is at least INTEL 2716 compatible. Each 2716 chip contains 16,384 bits of memory. The addressing of the chip is such that data is accessed eight bits at a time. The organization is 2048 bytes of eight bits each. A single 2716 provides 2K bytes of memory. The MEMORY PLUS board has provision for up to four 2716 chips providing for a maximum of 8K bytes of EPROM.

The 2716 chips required for MEMORY PLUS are INTEL 2716 or equivalent (not Texas Instrument 2716). This chip has the following basic parameters:

SPEED: 450 nanosecond access time
POWER: 105 milliamp worst case current, and
single +5 volt required

The MEMORY PLUS EPROM is organized into a single contiguous 8K block of memory. The location of the EPROM in the KIM-1 addressing space is defined by a switch which may be set to start at any 8K boundary (2K hex boundary). See the chart of switch positions on the preceding page. The position is determined by the flat section of the switch.

If, and only if, the "EK" address is used, then the jumper "J1" (located on the top side of component U4) must be changed. The existing jumper etched on the board must be cut and a wire run from the hole nearest the "J" to the hole nearest the "1". This will cause interrupts to be serviced by the FFFx vectors instead of the 1FFx KIM-1 vectors.

The EPROM sockets are addressed such that the socket nearest the edge of the board has the lowest address. The exact layout of the individual EPROM chips may be found in a diagram in the section on "MEMORY PLUS Testing and Field Repair".

VERSATILE INTERFACE ADAPTER

The MOS Technology 6522 Versatile Interface Adapter is one of the important pluses of MEMORY PLUS. This sophisticated chip has the following basic features:

I/O: Two 8-bit parallel I/O ports with additional handshaking control lines. This more than doubles the basic KIM-1 I/O capabilities.

TIMERS: Two powerful interval timers which have a number of operating modes permitting them to be used as counters, "free-running" timers, "one-shot" timers, and more.

SHIFT REGISTER: Perform serial I/O under control of a timer, the system clock or an external signal. Serial-to-parallel and parallel-to-serial conversions take place within the 6522 without involving the KIM-1 on a bit-by-bit basis.

INTERRUPTS: The many different devices on the 6522 can cause interrupts to signal the completion of activity. These interrupts can be individually enabled, disabled and tested.

The 6522 chip has two functions on MEMORY PLUS. The first is to provide all of the 6522 capabilities to the user as an extension of the KIM-1. The second is to control the EPROM Programmer. The 6522 is the heart of the EPROM Programmer. When the system is being used to program EPROMs, then the 6522, as well as several I/O lines from the basic KIM-1, is dedicated to this task. See the section on "EPROM Programming" for details.

The addressing of the 6522 is determined by the K5 signal generated by the KIM-1, and the AB8 and AB9 address signals. The sixteen internal registers of the 6522 have the following addresses and functions:

1600	ORB	Output Register B/Input Register B
1601	ORA	Output Register A/Input Register A With Handshake
1602	DDRB	Data Direction Register B
1603	DDRA	Data Direction Register A
1604	T1C-L	Timer/Counter 1 Low
1605	T1C-H	Timer/Counter 1 High
1606	T1L-L	Timer/Counter 1 Low
1607	T1L-H	Timer/Counter 1 High
1608	T2C-L	Timer/Counter 2 Low
1609	T2C-H	Timer/Counter 2 High
160A	SR	Shift Register
160B	ACR	Auxiliary Control Register
160C	PCR	Peripheral Control Register
160D	IFR	Interrupt Flag Register
160E	IER	Interrupt Enable Register
160F	ORA2	Output Register A/Input Register A Without Handshake

See the "MCS6522 VERSATILE INTERFACE ADAPTER" Preliminary Data Sheet included with this documentation for details on the 6522 operations.

EPROM Programming

The usefulness of the EPROMs on the MEMORY PLUS board is enhanced by the inclusion of on board EPROM programming facilities. The INTEL 2716 EPROM is electrically programmable and ultraviolet light erasable. The user can buy or build an ultraviolet light eraser. MEMORY PLUS provides the parts required for the programming of the EPROMs. These parts consist of the following items:

EPROM Programming Socket: Socket 79 is a 24 pin socket located toward the lower right hand corner of the board. The EPROM to be programmed is placed in this socket.

+25 Volt Regulator: +25 volts is required for programming the 2716. This may be provided directly by the user at pin A-22 of the MEMORY PLUS application connector. Since this voltage is so critical, and since an over voltage can destroy an EPROM, an on board regulator circuit is provided. This will provide about 24.7 volts when supplied with +27 to +30 volts at pin E-3 of the MEMORY PLUS expansion connector.

Control Lines: The EPROM requires eleven (11) address lines, eight (8) data lines, and two (2) control lines. All but three of these lines are provided by the MEMORY PLUS VIA 6522. The remaining three lines come from the KIM-1 port B: PB0, PB1, and PB2.

Timing: EPROM programming requires a 50 millisecond pulse be applied to the EPROM. The VIA 6522 includes a timer which is used for timing this interval.

EPROM Programming Program: The control of the programming is handled by a program run on the KIM-1. This program is provided in the form of a source listing in this manual and as a cassette tape included in the MEMORY PLUS package.

The 2716 EPROM may be programmed one location (byte) at a time, or the entire EPROM may be programmed. The steps required to program the EPROM are:

1. With the power off, insert the EPROM to be programmed into the Programming Socket.

2. Turn on the power and load the data to be copied into the EPROM into any portion of memory. This may be RAM memory loaded from cassette (or by hand) or may be another EPROM which is going to be copied.

3. Load the EPROM Programming Program from cassette (or by hand) into memory (locations 0000 to 0094)

4. Make sure the following application connector connections are in place: KIM A-9 to MP A-19; KIM A-10 to MP A-20; KIM A-11 to MP A-21; KIM A-H to MP A-L.

5. Set up the following parameters for the EPROM Programming Program:

0000 and 0001	Starting address of memory to be copied from.
0002 and 0003	First address in EPROM to be copied to.
0004 and 0005	Last address +1 of memory to be copied from.

For example, to copy from RAM locations 2000 through 217A into the EPROM starting at location 0300, the following values would be set:

0000	00	Low byte of Starting address 2000
0001	20	High byte of Starting address 2000
0002	00	Low byte of First address in EPROM 0300
0003	03	High byte of First address in EPROM 0300
0004	7B	Low byte of Last address +1 217A = 7B
0005	21	High byte of Last address +1 217A

6. Turn on +25 volt supply connected to MP A-22 or unregulated +27 to +30 volt supply connected to MP E-3.

7. Set the program starting address of 0006 via the keypad or the terminal and then press GO or type G.

8. It will take about 50 milliseconds per location for programming. This means about 100 seconds to program an entire 2K EPROM. When the program is done it will return to the KIM Monitor with address 0081 and data 1C. This indicates successful completion of the requested programming.

9. Turn off the +25 volt (or +27 to +30 volt) supply and the rest of the power to the system. Then remove the EPROM from the programming socket. The EPROM may now be placed in its operational socket and used.

10. The EPROM Programming Program performs several tests and may exit to the KIM Monitor at a location other than 0081 to indicate an error.

    0067 A Verify error. The correct data has not been programmed into the EPROM. This may be caused by:

    An EPROM which was not "clean" (all 1's) to start.
    A defective EPROM.
    One or more address lines from the KIM-1 not properly hooked up or not properly functioning.

    0072 A Starting address error. The memory address pointer has tried to go beyond location FFFF. This may be caused by:

    Providing an incorrect Starting address in locations 0000 and 0001.
    Providing an incorrect Last address in locations 0004 and 0005.

    008C An EPROM address error. The EPROM address pointer has tried to go beyond location FFFF. This may be caused by:

    Providing an incorrect First address in locations 0002 and 0003.
    Providing an incorrect Last address in locations 0004 and 0005.

The following connections must be made between the KIM-1 and the MEMORY PLUS board before any EPROM Programming can take place:

KIM A-9 to MP A-19	Port B Bit 0 (PB0)	Address Bit 8 for EPROM
KIM A-10 to MP A-20	Port B Bit 1 (PB1)	Address Bit 9 for EPROM
KIM A-11 to MP A-21	Port B Bit 2 (PB2)	Address Bit 10 for EPROM
KIM A-H to MP A-L	K5 which is used in conjunction with the address bus to select the VIA at addresses 160x.	

If the MEMORY PLUS board is mounted in its normal position, directly below the KIM-1, it may be difficult or impossible to get access to the EPROM socket for programming. There are two ways around this problem.

1. Use a 24 pin header to bring wires directly from the EPROM Programming Socket out to a more accessible location.

2. Attach wires for an additional EPROM Programming Socket directly to the MP application connector. All of the lines necessary for attaching an external EPROM Programming Socket are available:

EPROM Socket	MP Application Connector	Function
1	A-15	Address bit 7 from VIA PB7
2	A-B	Address bit 6 from VIA PB6
3	A-16	Address bit 5 from VIA PB5
4	A-13	Address bit 4 from VIA PB4
5	A-12	Address bit 3 from VIA PB3
6	A-11	Address bit 2 from VIA PB2
7	A-10	Address bit 1 from VIA PB1
8	A-9	Address bit 0 from VIA PB0
9	A-14	Data bit 0 from VIA PA0
10	A-2	Data bit 1 from VIA PA1
11	A-3	Data bit 2 from VIA PA2
12	A-1	Ground
13	A-4	Data bit 3 from VIA PA3
14	A-5	Data bit 4 from VIA PA4
15	A-6	Data bit 5 from VIA PA5
16	A-7	Data bit 6 from VIA PA6
17	A-8	Data bit 7 from VIA PA7
18	A-18	Program Pulse Inverted from VIA CB2
19 [KIM A-11]	A-21	Address bit 10 from KIM PB2
20	A-F	Chip Select from VIA CA2
21	A-22	+25V direct or from +27 to +30 regulator
22 [KIM A-10]	A-20	Address bit 9 from KIM PB1
23 [KIM A-9]	A-19	Address bit 8 from KIM PB0
24 [KIM A-A]	A-A	+5V regulated

The addressing for the EPROM Socket only consists of eleven (11) bits. This means that addressing for programming purposes runs from 0000 to 07FF, regardless of the actual address that the EPROM will eventually reside at. The high order five (5) bits of EPROM address are totally defined by which socket the EPROM is placed in and where the set of EPROMs are switched to: 2000, 4000,..., E000.

```
                        PROM PROGRAMMER  29 MAY 1978

                        PROM    ORG     $0000

                        ORB     *       $1600   OUTPUT REGISTER B
                        ORA     *       $1601   OUTPUT REGISTER A
                        DDRB    *       $1602   DATA DIRECTION REGISTER B
                        DDRA    *       $1603   DATA DIRECTION REGISTER A
                        TTWOL   *       $1608   TIMER TWO LOW
                        TTWOH   *       $1609   TIMER TWO HIGH
                        PCR     *       $160C   PERIPHERAL CONTROL REGISTER
                        IFR     *       $160D   INTERRUPT FLAG REGISTER
                        IER     *       $160E   INTERRUPT ENABLE REGISTER

                        PBD     *       $1702   PORT B DATA ON KIM-1
                        PBDD    *       $1703   PORT BE DATA DIRECTION

                        MONTOR  *       $1C05   KIM MONITOR ENTRY

0000 00                 SAL     =       $00     STARTING ADDRESS LOW
0001 00                 SAH     =       $00     STARTING ADDRESS HIGH
0002 00                 PRMLOW  =       $00     EPROM LOW ADDRESS
0003 00                 PRMHGH  =       $00     EPROM HIGH ADDRESS
0004 00                 EAL     =       $00     END ADDRESS LOW
0005 00                 EAH     =       $00     END ADDRESS HIGH

0006 A9 00              SETUP   LDAIM   $00     CLEAR ALL STATUS BITS
0008 48                         PHA             BY PUSHING 00 ON STACK
0009 28                         PLP             AND POPPING TO STATUS
000A A9 8D                      LDAIM   INTRPT  SET INTERRUPT VECTOR TO
000C 8D FE 17                   STA     $17FE   POINT TO INTERRUPT ROUTINE
000F A9 00                      LDAIM   INTRPT  / PAGE NUMBER
0011 8D FF 17                   STA     $17FF
0014 A9 7F                      LDAIM   $7F     DISABLE INTERRUPTS
0016 8D 0E 16                   STA     IER
0019 A9 FF                      LDAIM   $FF     CLEAR INTERRUPTS PENDING
001B 8D 0D 16                   STA     IFR
001E A9 A0                      LDAIM   $A0     NOW ENABLE TIMER TWO
0020 8D 0E 16                   STA     IER
0023 A9 EC                      LDAIM   $EC     SET PROGRAM LOW, VERIFY MODE
0025 8D 0C 16                   STA     PCR

0028 A9 FF              NEXT    LDAIM   $FF     SET DATA DIRECTION
002A 8D 02 16                   STA     DDRB    REGISTERS FOR OUTPUT
002D 8D 03 16                   STA     DDRA
0030 8D 03 17                   STA     PBDD
0033 A5 02                      LDAZ    PRMLOW  OUTPUT NEXT EPROM ADDRESS
0035 8D 00 16                   STA     ORB     LOW VIA ORB
0038 A5 03                      LDAZ    PRMHGH  OUTPUT HIGH PROM ADDRESS
003A 8D 02 17                   STA     PBD     VIA PBD
003D A0 00                      LDYIM   $00     GET BYTE OF DATA
003F B1 00                      LDAIY   SAL     VIA POINTERS
0041 8D 01 16                   STA     ORA     OUTPUT VIA ORA

0044 A9 50              TIMER   LDAIM   $50     SETUP 50 MILLISECOND TIMER
0046 8D 08 16                   STA     TTWOL   OUTPUT TO TIMER TWO LOW
```

```
0049 A9 C3          LDAIM $C3    SECOND BYTE OF TIMING COUNT
004B 8D 09 16       STA   TTWOH  OUTPUT TO TIMER TWO HIGH
004E A9 CE          LDAIM $CE    SET PROGRAM HIGH, PROGRAM MODE
0050 8D 0C 16       STA   PCR    START PROGRAMMING

0053 C0 00     WAIT CPYIM $00    TEST FOR INTERRUPT SERVICED
0055 F0 FC          BEQ   WAIT   ELSE, WAIT FOR IT

0057 A9 00     VERIFY LDAIM $00  VERIFY PROGRAMMING
0059 8D 03 16       STA   DDRA   SET ORA FOR INPUT
005C A0 00          LDYIM $00    SETUP POINTER
005E AD 01 16       LDA   ORA    READ FROM PROM
0061 D1 00          CMPIY SAL    COMPARE
0063 F0 03          BEQ   OKAY   GOOD IF MATCH
0065 20 05 1C       JSR   MONTOR ELSE PROM ERROR

0068 E6 00     OKAY INCZ  SAL    BUMP DATA POINTER
006A D0 07          BNE   TEST   BRANCH IF NOT ZERO
006C E6 01          INCZ  SAH    BUMP HIGH DATA POINTER
006E D0 03          BNE   TEST   BRANCH IF NOT ZERO
0070 20 05 1C       JSR   MONTOR ELSE BAD

0073 A5 05     TEST LDAZ  EAH    TEST ALL DONE
0075 C5 01          CMPZ  SAH    BY COMPARING SAL,SAH AND
0077 D0 09          BNE   MORE   EAL,EAH VECTORS
0079 A5 04          LDAZ  EAL
007B C5 00          CMPZ  SAL
007D D0 03          BNE   MORE
007F 20 05 1C       JSR   MONTOR

0082 E6 02     MORE INCZ  PRMLOW BUMP PROM POINTERS
0084 D0 A2          BNE   NEXT   READY IF NOT ZERO
0086 E6 03          INCZ  PRMHGH BUMP HIGH POINTER
0088 D0 9E          BNE   NEXT   OKAY IF NOT ZERO
008A 20 05 1C       JSR   MONTOR ERROR

008D AC 0D 16  INTRPT LDY  IFR    CLEAR INTERRUPT
0090 8C 0D 16       STY   IFR    VIA SNEAKY TRICK
0093 A0 EC          LDYIM $EC    RESET PROGRAM LOW, VERIFY MODE
0095 8C 0C 16       STY   PCR
0098 40             RTI          RETURN FROM INTERRUPT
```

```
SYMBOL TABLE
DDRA   1603   DDRB   1602   EAH    0005   EAL    0004
IER    160E   IFR    160D   INTRPT 008D   MONTOR 1C05
MORE   0082   NEXT   0028   OKAY   0068   ORA    1601
ORB    1600   PBDD   1703   PBD    1702   PCR    160C
PRMHGH 0003   PRMLOW 0002   PROM   0000   SAH    0001
SAL    0000   SETUP  0006   TEST   0073   TIMER  0044
TTWOH  1609   TTWOL  1608   VERIFY 0057   WAIT   0053
```

MEMORY PLUS Testing and Field Repair

Your MEMORY PLUS board has been burned in and tested before shipment. If, after following the steps outlined in the "Setting Up MEMORY PLUS" section, the board does not seem to work properly, or if it ever seems to stop functioning correctly, then the following steps should be taken.

1. Check that the board is receiving adequate power.

   Place the ground lead of a voltmeter or 'scope on any convenient ground on the board (the left lead of the large capacitor at the upper left hand corner of the board is handy) or on the connector (A-1, E-1, E-22, E-A, or E-Z).

   Measure the +5 volts at each of the four jumpers on the Header located near the voltage regulators. If you are providing unregulated +8 to +10 volts, then the top jumper should have this value. If you are using regulated +5 volts, then the top jumper should show +5V. The bottom three jumpers should show +5V in any case. If not, check your supply. If one of the three shows a voltage other than +5, it indicates a problem with the associated voltage regulator which might require replacement. The bottom jumper comes from Q6, the next jumper from Q5, and the next to top jumper from Q4. (See diagram on page 23).

   Measure the +25 volts at pin A-22 of the MEMORY PLUS application connector. If you are providing unregulated +27 to +30 volts, the output of the +25 volt regulator circuit should show about +24.7V. If you are providing regulated +25 volts at this pin, it will show the output of your power supply. If the value for the unregulated situation is not +24.7, then check your unregulated voltage at pin E-2 of the MEMORY PLUS expansion connector. It must be +27 to +30V.

2. Check that all IC chips are firmly in their sockets. It is possible for chips to come loose during handling and shipping. Push each chip firmly into its socket.

3. Check that the Header is in the proper position for the method of providing +5 volts. If you are providing +5 at pins E-21 and E-Y, then the Header should have its notched corner at pin 9 and the jumper wires should go from pins 2 - 15, 4 - 13, 6 - 11, and 8 - 9. If you are providing unregulated +8 to +10 volts at pins E-19 and E-20, then the Header should have its notched corner at pin 1 and the jumper wires should go from pins 1 - 16, 3 - 14, 5 - 12, and 7 - 10.

4. Check all of the connections between the KIM-1, MEMORY PLUS, and the power supplies.

5. Follow the instructions in the "RAM Memory Test" section if the RAM Memory appears to be having problems.

6. Check the KIM-1 or try MEMORY PLUS with a different KIM-1. For EPROM Programming it is absolutely essential that bits 0, 1, and 2 of the KIM-1 Port B are functioning properly (PB0, PB1, and PB2). A quick test of Port B may be made by putting FF in location 1703 and then trying to write 07 in location 1702. If this does not work, then you have a problem and should <u>not</u> attempt to program any EPROMs until you have the KIM-1 serviced.

Remember that you are exercising your KIM-1 in ways you may have never tried before. This will, in some cases, uncover faults that have existed undetected in a KIM-1. For example, my own "reliable" KIM-1 which I have been using extensively for well over a year, turned out to have a defective Port B. Bits 0 and 1 which I had been using for cassette control worked fine, but bit 2 did not. I zapped a few EPROMs, not fatally thank goodness, before discovering this. Another KIM-1 I used had flakey memory in Page Zero such that the RAM Memory Test would not work. So, it really can happen.

7. Check all MEMORY PLUS switches and jumpers. In addition to the Header which was discussed in 1. and 3. above, there are two switches and a jumper to be concerned with:

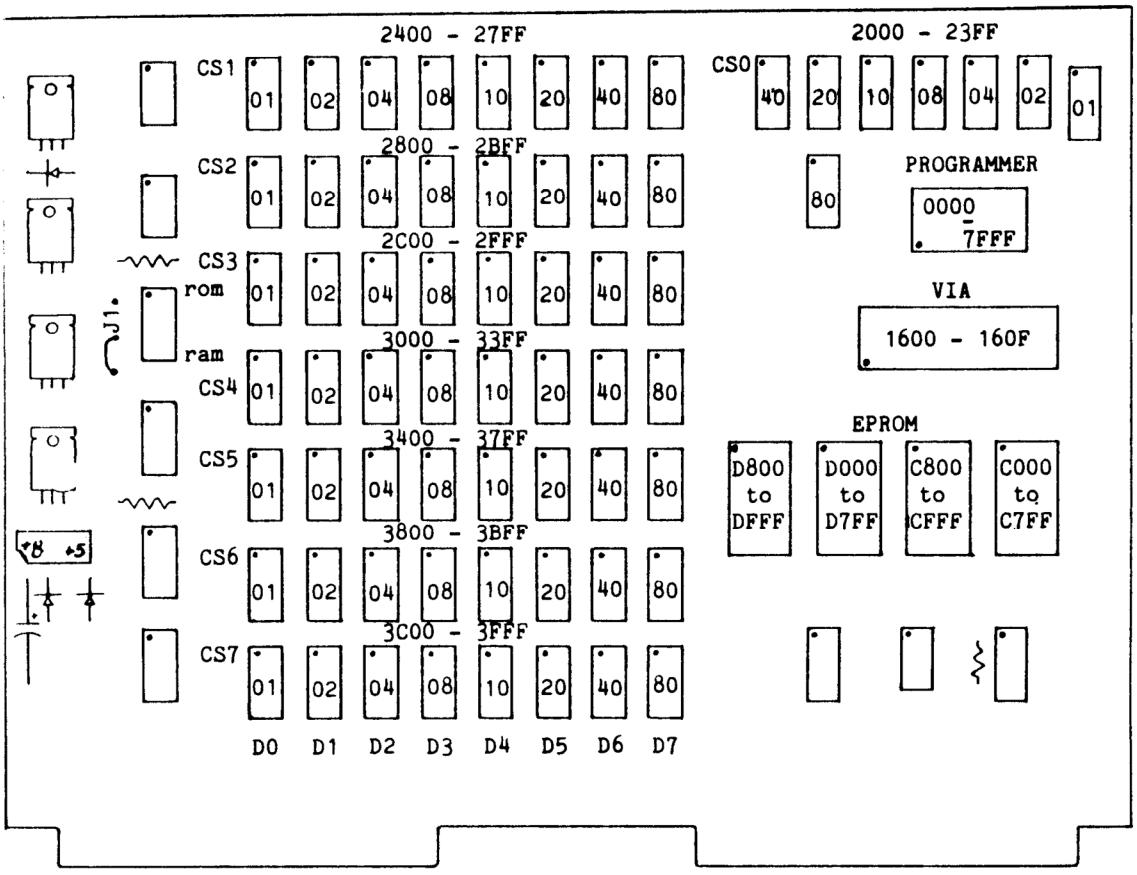
   The RAM Address Select Switch (see page 8) must be set to "2K" for the Memory Test to work as documented. Actually, the memory test will work with any addresses, as long as the correct parameters are set in page zero location 0000 - start page number = first page to test and location 0001 - end page number = last page to test. The RAM switch must be selecting the bank of memory you are attempting to test, and it may not be selecting the same chunk of memory as the ROM select switch.

   The ROM Address Select Switch (see page 8) must not be set to the same starting address as the RAM switch. If the ROM switch is set to "EK", then there will be conflict with the KIM-1 Monitor interrupt vectors unless the jumper changes discussed on page 9 have been made, since the board comes with the jumper set so that interrupts will be decoded by the KIM-1 Monitor locations 1FFA through 1FFF. If you put ROM in E000 to FFFF, then this jumper must be changed. Otherwise any address in this range will be decoded twice: as E000 to FFFF and 0000 to 1FFF.

8. Check that all EPROMs are inserted in the proper direction. Pin 1 in the EPROM Programming Socket is in the upper left corner. Pin 1 in the EPROM normal sockets is in the upper right corner.

MEMORY PLUS was designed for easy field repair. It is, of course, hoped that no repair will ever be required on your unit. If some repair is required, then it is hoped that it can be done by the user or some local source. The unit should only have to be sent back for factory servicing in rare circumstances. This means that your MEMORY PLUS board should never be down very long.

Memory Organization with RAM selected at "2K" and ROM selected at "CK".



The dot in one corner of each IC chip and Header indicates the proper location of pin 1. The Header has two corners marked, one labelled +5 and one labelled +8. These indicate the proper orientation of the Header when the power supply is providing a regulated +5 volts or an unregulated +8 to +10 volts.

ROM and RAM show the location of the switches used to select the base address for the ROM and RAM memories.

J1 marks the location of the jumper which must be changed if ROM is placed to start at E000. The line shown is the etched jumper which causes interrupt addresses (FFFA to FFFF) to select the KIM-1 Monitor interrupt vectors (1FFA to 1FFF). This jumper must be removed and replaced by a jumper from the dot near the J to the dot near the 1 if interrupts are to be decoded by the high addresses.

RAM Memory Test

You should test the MEMORY PLUS RAM when you initially set up your system. You may also want to test it from time-to-time to make sure it is all still working properly. And, of course, you will want to test it whenever you have any reason to suspect that it may not be working right. The following memory test is copied from the work cited under "NOTES" on page 22.

"Testing RAM isn't just a question of storing a value and then checking it. It's important to test for interference between locations. Such tests often involve writing to one location and then checking all other locations to see they haven't been disturbed; this can be time consuming.

This program checks memory thoroughly and runs exceptionally fast. It is adapted from an algorithm by Knaizuk and Hartmann published in "IEEE Transactions on Computers", April 1977.

The program first puts value FF in every location under test. Then it puts 00 in every third location, after which it tests all locations for correctness. The test is repeated twice more with the positions of the 00's changed each time. Finally, the whole thing is repeated with the FF and 00 values interchanged.

To Run: Set the addresses of the first and last memory pages you wish to test into locations 0000 and 0001 respectively. Start the program at address 0002; it will halt with a memory address on the display. If no faults were found, the address will be one location past the last address tested. If a fault is found, its address will be displayed."

The MEMORY PLUS version of the memory test is set up to test from page 20 (2000 hex) through page 3F (3FFF hex). After loading the program from the cassette tape (or by hand), set address 0003 and press GO. If the memory checks out completely, then after a few seconds the display will show the address 4000 in the address portion of the display. If an error is detected, then the address containing the error will be displayed. Since the program will halt at the first detected error, there is no way to test for additional errors within a page beyond the first error. You can test other pages by changing the starting and ending page addresses in locations 0000 and 0001, and run the test multiple times by setting location 0003 to 02 through 0F. The rightmost digit on the display will downcount the passes through the test until 00 is reached.

Once a bad location has been detected, you can examine the location via the KIM Monitor and perhaps determine the problem. For example, if the location has a data value of 7F, it would indicate that the most significant bit was not working. Refering to the Memory Organization drawing you could determine which 2102 chip was responsible for this bit. Since the RAM chips are all socketted, it is a simple matter to remove the suspect chip and replace it with another chip. Even if you do not have any spare 2102 chips handy, you can swap the suspect chip with another chip and see if the problem moves with the chip or stays in the same location. IMPORTANT NOTE: Turn the power off when removing any chips, otherwise you may destroy the memory chips. If the problem moves with the chip, then the solution is to get a replacement chip. If the problem does not move with the chip, then you must look elsewhere for the solution.

The next test would be to swap the 74LS367 chips and see if the problem shifted. Then the 74LS138 chips could be swapped. Finally you could replace the 74LS00, 74LS32, or 74LS04 chips. Note that the replacements do not have to be "LS" type. One of the above chip replacements should solve 99% of the problems which occur in the field.

```
                    MEMORY TEST - 15 MAY 1978

                    BASED ON "MEMORY TEST" BY JIM BUTTERFIELD IN
                    "THE FIRST BOOK OF KIM".

                    MEMORY ORG   $0000

                    POINTL *     $00FA
                    POINTH *     $00FB  DISPLAY POINTERS
                    SAD    *     $1740  DISPLAY DATA REGISTER
                    SADD   *     $1741
                    SBD    *     $1742  DISPLAY DIGIT REGISTER
                    SBDD   *     $1743
                    GOKIM  *     $1C4F  ENTRY INTO KIM MONITOR
                    TABLE  *     $1FE7  DISPLAY CONVERSION TABLE IN KIM

0000 20             BEGIN  =     $20    STARTING PAGE FOR TEST
0001 3F             END    =     $3F    ENDING PAGE FOR TEST
0002 05             TIMES  =     $05    NUMBER OF PASSES THROUGH TEST

0003 A9 7F      START  LDAIM $7F    SET UP DATA DIRECTION PORTS
0005 8D 41 17          STA   SADD   FOR OUTPUT TO DISPLAY
0008 A9 1E             LDAIM $1E
000A 8D 43 17          STA   SBDD
000D A9 12             LDAIM $12    SELECT RIGHTMOST DIGIT
000F 8D 42 17          STA   SBD    OF KIM DISPLAY FOR COUNTER
0012 A5 02             LDAZ  TIMES  SETUP COUNTER
0014 85 92             STAZ  TCOUNT
0016 A9 00             LDAIM $00    ZERO POINTERS
0018 48                PHA          CLEAR STATUS FLAGS
0019 28                PLP          BY PUSHING ZERO ON STACK
001A A8                TAY          AND PULLING TO STATUS
001B 85 FA             STAZ  POINTL

001D 85 90      BIGLP  STAZ  FLAG   = 00 FIRST PASS, = FF SECOND PASS
001F A6 92             LDXZ  TCOUNT DISPLAY COUNTER
0021 BD E7 1F          LDAX  TABLE  AFTER CONVERSION TO SEGMENTS
0024 8D 40 17          STA   SAD
0027 A2 02             LDXIM $02    SET 3 TESTS EACH PASS
0029 86 91             STXZ  PASS

002B A5 00      NPASS  LDAZ  BEGIN  SET POINTER TO
002D 85 FB             STAZ  POINTH START OF TEST AREA
002F A6 01             LDXZ  END
0031 A5 90             LDAZ  FLAG
0033 49 FF             EORIM $FF    REVERSE FLAG
0035 85 8F             STAZ  FLIP   = FF FIRST PASS, 00 SECOND PASS

0037 91 FA      CLEAR  STAIY POINTL WRITE FLIP VALUE
0039 C8                INY         INTO ALL LOCATIONS
003A D0 FB             BNE   CLEAR
003C E6 FB             INCZ  POINTH
003E E4 FB             CPXZ  POINTH
0040 B0 F5             BCS   CLEAR

                    FLIP VALUE IN ALL LOCATIONS.  NOW CHANGE 1 IN 3

0042 A6 91             LDXZ  PASS
0044 A5 00             LDAZ  BEGIN  SET POINTER
0046 85 FB             STAZ  POINTH BACK TO START
```

```
0048 A5 90      FILL    LDAZ  FLAG    CHANGE VALUE
004A CA         TOP     DEX
004B 10 04              BPL   SKIP    SKIP 2 OUT OF 3
004D A2 02              LDXIM $02     RESTORE 3 COUNTER
004F 91 FA              STAIY POINTL  CHANGE 1 OF 3
0051 C8         SKIP    INY
0052 D0 F6              BNE   TOP
0054 E6 FB              INCZ  POINTH  NEW PAGE
0056 A5 01              LDAZ  END     HAVE WE PASSED
0058 C5 FB              CMPZ  POINTH  END OF TEST AREA?
005A B0 EC              BCS   FILL    NO.  KEEP GOING

                MEMORY SET UP.  NOW TEST IT.

005C A5 00              LDAZ  BEGIN   SET POINTER BACK
005E 85 FB              STAZ  POINTH  TO START
0060 A6 91              LDXZ  PASS    SET UP 3 COUNTER

0062 A5 8F      POP     LDAZ  FLIP    TEST FOR FLIP VALUE
0064 CA                 DEX           2 OUT OF 3 TIMES
0065 10 04              BPL   SLIP    OR
0067 A2 02              LDXIM $02     1 OUT OF 3 TIMES
0069 A5 90              LDAZ  FLAG    TEST FOR FLAG VALUE
006B D1 FA      SLIP    CMPIY POINTL  HERE IS THE TEST
006D D0 1B              BNE   OUT     BRANCH IF FAILED
006F C8                 INY           BUMP POINTER
0070 D0 F0              BNE   POP     IF NOT DONE KEEP GOING
0072 E6 FB              INCZ  POINTH
0074 A5 01              LDAZ  END     TEST END
0076 C5 FB              CMPZ  POINTH
0078 B0 E8              BCS   POP

                ABOVE TEST OKAY.  CHANGE AND REPEAT

007A C6 91              DECZ  PASS    CHANGE 1 IN 3 POSITION
007C 10 AD              BPL   NPASS   AND DO NEXT PASS
007E A5 90              LDAZ  FLAG    INVERT FLAG
0080 49 FF              EORIM $FF     FOR PASS TWO
0082 30 99              BMI   BIGLP   AND REPEAT BIG LOOP
0084 84 FA              STYZ  POINTL  SAVE LOW ORDER ADDRESS
0086 C6 92              DECZ  TCOUNT  DECR. TIMES COUNTER
0088 D0 93              BNE   BIGLP   IF NOT TO ZERO, GO AGAIN

008A 84 FA      OUT     STYZ  POINTL  PUT LOW ORDER ADDRESS TO
008C 4C 4F 1C           JMP   GOKIM   DISPLAY AND GO TO KIM

008F 00         FLIP    =     $00
0090 00         FLAG    =     $00
0091 00         PASS    =     $00
0092 00         TCOUNT  =     $00


SYMBOL TABLE
BEGIN   0000    BIGLP   001D    CLEAR   0037    END     0001
FILL    0048    FLAG    0090    FLIP    008F    GOKIM   1C4F
MEMORY  0000    NPASS   002B    OUT     008A    PASS    0091
POINTH  00FB    POINTL  00FA    POP     0062    SADD    1741
SAD     1740    SBDD    1743    SBD     1742    SKIP    0051
SLIP    006B    START   0003    TABLE   1FE7    TCOUNT  0092
TIMES   0002    TOP     004A
```

MEMORY PLUS Parts List

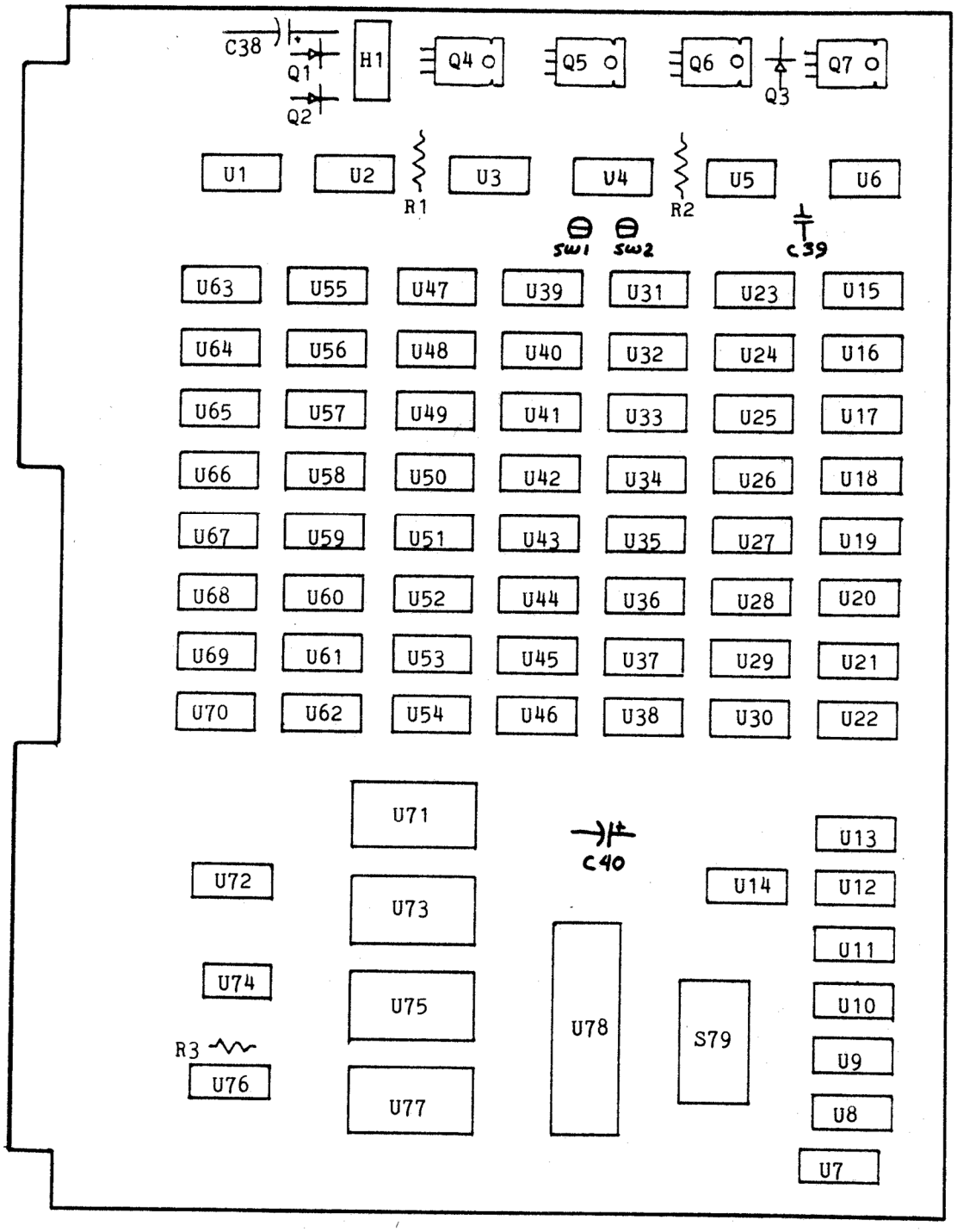
ITEM	PART	Qty.	DESCRIPTION
1.	U1, U2, U72	3	IC 74LS367 Hex Bus DRiver with 3-state outputs
2.	U3, U4, U76	3	IC 74LS138 3-to-8 Line Decoder
3.	U5	1	IC 74LS00 Quad 2-Input Positive NAND Gates
4.	U6	1	IC 74LS32 Quad 2-Input Positive OR Gates
5.	U74	1	IC 74LS04 Hex Inverter
6.	U7 - U70	64	Memory Element 2102 450 nanosec, low power
7.	SW1, SW2	2	1-of-7 Rotary Switch
8.	R1 - R3	3	Resistor 3.3K, 1/4 watt
9.	C1 - C37	37	Capacitor .01 MFD, 50WV DC
10.	C38	1	Electrolytic Capacitor 22 - 25 MFD, 25V
11.	C39	1	Capacitor .001 MFD
12.	C40	1	Electrolytic Capacitor 3 - 5 MFD, 35V
13.	Q1, Q2, Q3	3	Diodes 1N4001 Rectifier 50V
14.	Q4, Q5, Q6	3	Voltage Regulator LM340T-5, +5V, 1.0A
15.	Q7	1	Voltage Regulator LM340T-24, +24V, 1.0A
16.	HS1 - HS3	3	T220 Heat Sink (Large)
17.	HS4	1	T220 Heat Sink (Small)
18.	S1 - S4, S7 - S70, S72, S76, S80	71	IC Socket 16 pin
19.	S5, S6, S74	3	IC Socket 14 pin
20.	S71, S73, S75, S77, S79	5	IC Socket 24 pin
21.	S78	1	IC Socket 40 pin
22.	H1	1	IC Socket Header 16 pin
23.	U78	1	VIA 6522 Versatile Interface Adapter
	Accessories Package		
24.		3	Connector 44 pin (dual 22) (NOT included if a Cable has been ordered.)
25.		3	Battery Clip 9V transistor battery type
26.			Misc. Hardware

NOTES:

1. The Memory Test is adapted from "Memory Test" by Jim Butterfield which appears on pages 122 and 123 of THE FIRST BOOK OF KIM, edited by Butterfield, Ockers and Rehnke, published by Hayden Book Company. The book sells for $9.00 and is a must for any 6502 user.

2. The program listings in this manual were produced by the Micro-ADE Assembler on a KIM-1 with a MEMORY PLUS board. The COMPUTERIST version of Micro-ADE includes a cassette tape with two versions of Micro-ADE. One has the program in 2000 to 2FFF and uses 3000 to 3FFF for the Source and Symbol working areas. The other has the program in C000 to CFFF and uses 2000 to #FFF for the Source and Symbol working areas. This second version is ready to be placed into EPROM and left resident in your MEMORY PLUS board. Micro-ADE costs $25.00 for the Operators Manual and Cassette Tape. This Manual includes most of the Input/Output Source Listings so that the user can customize the package to his type of terminal. Complete Source Listings are available for an additional $25.00.

MEMORY PLUS Component Layout



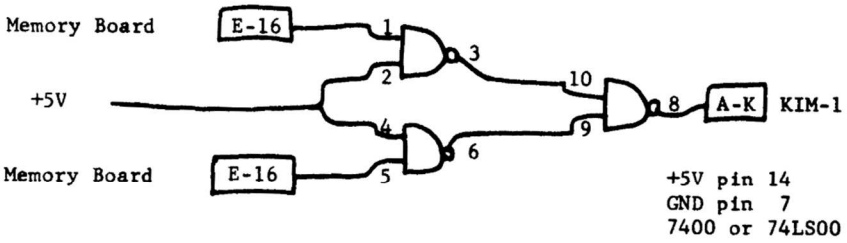
Application Note #1

Adding Multiple Memory Boards

Adding multiple memory boards, be they MEMORY PLUS or a mixture of MEMORY PLUS and KIM-2 or KIM-3's, is quite straightforward. Memory boards may be either connected directly to the KIM or may be connected via a bus driver/receiver such as the KIM-4.

Adding Multiple Memory Boards without a bus interface:

1. Keep the connecting leads as short as possible (6-8" maximum).
2. Bus the GROUND with heavy wire (eg. 18 gauge) because power supply currents as well as signals must be transmitted. This is a common cause of problems in microprocessor systems.
3. If the multiple memory boards are all <u>always</u> going to be in the system, then use the DECODE output from any <u>one</u> of them to drive the KIM-1 via pin K of the KIM-1 application connector. The DECODE output of Memory Plus, KIM-2, or KIM-3 is pin 16 of the memory expansion connector. On Memory Plus this signal is called DECODE and is also available at pin K of the application connector. On the KIM-2/KIM-3 boards this signal is called BOARD SELECT.
4. If the configuration of memory boards is going to change from time-to-time, then every board should have its DECODE connected to the KIM-1 so that whatever board is in the system will be able to generate the DECODE. To accomplish this, the DECODE signals from each memory board connector must be OR'd together so that the KIM-1 receives one signal. See the following diagram:

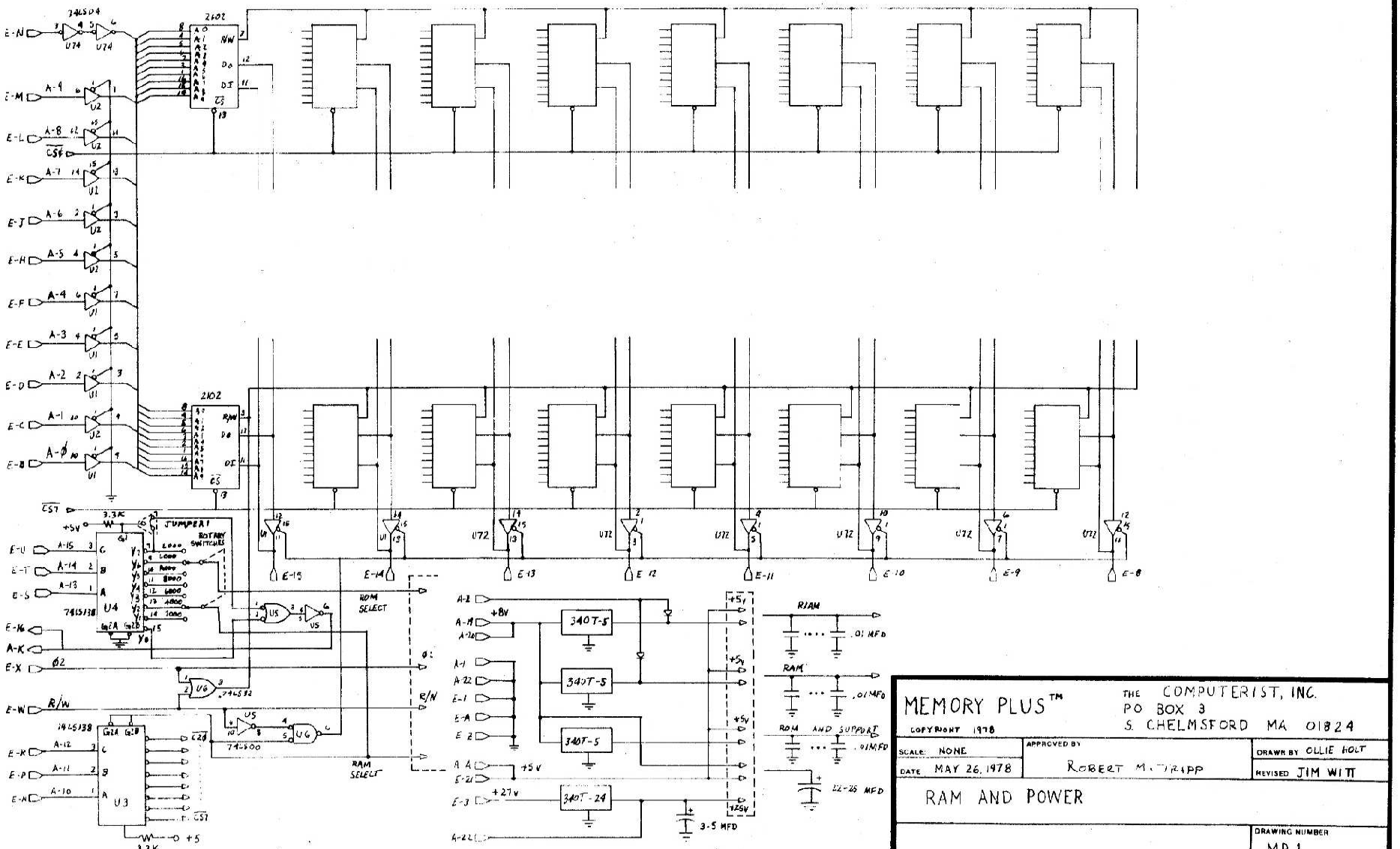


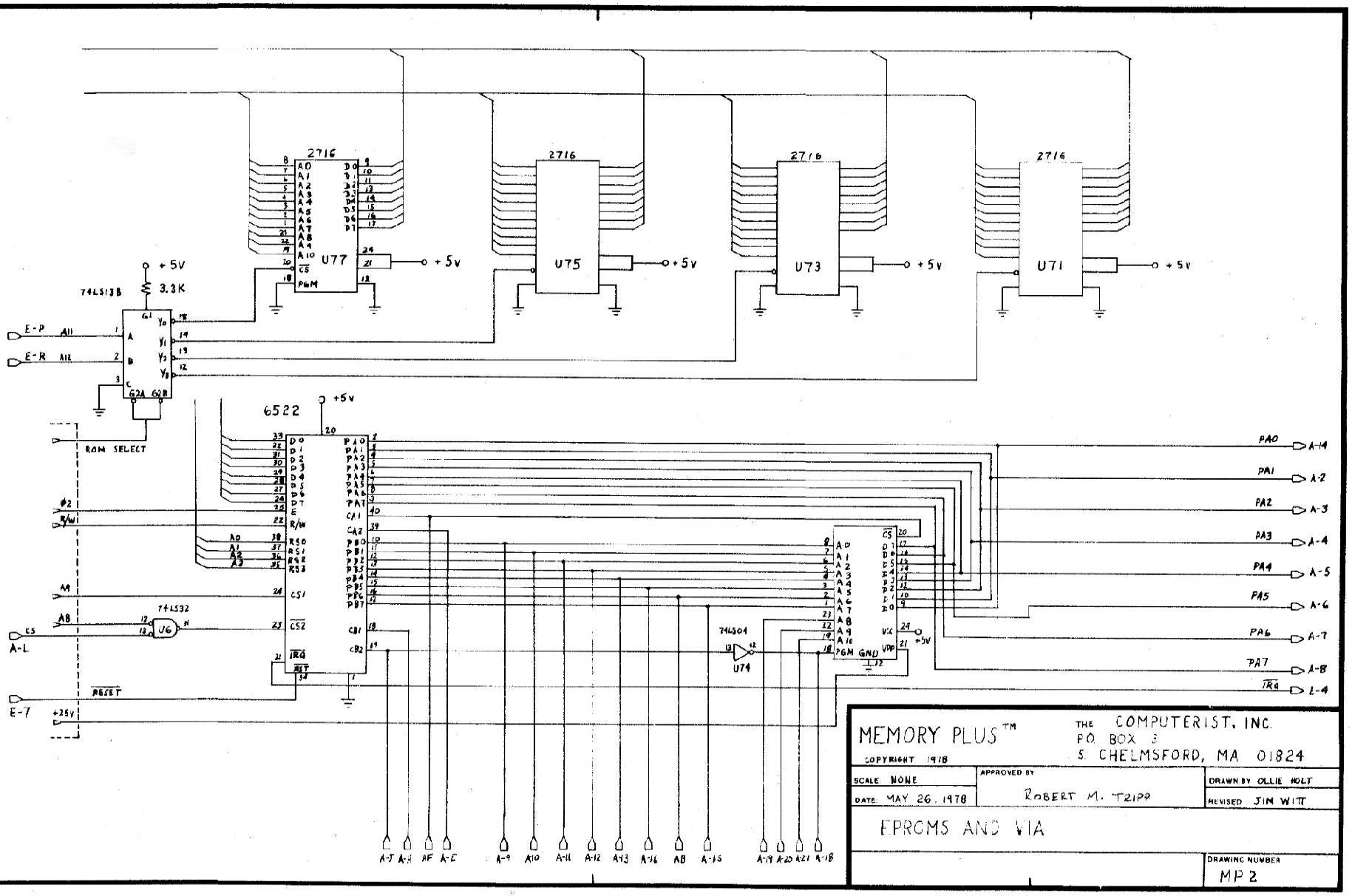
Adding Multiple Memory Boards with KIM-4 bus interface:

1. Do not connect DECODE to anything. The KIM-1 memory is selected by logic on the bus interface.
2. Make sure that Memory Plus's +5V BATTERY and +27V UNREG. lines don't get connected to the KIM-4 bus. Traces must be cut on one board or the other.

Limitations:

1. The limiting factor on adding boards is the drive of the KIM-1. This is capable of driving at least two memory boards. Three or more boards may require additional buffering between the KIM-1 and the memory boards.
2. Each 6522 VIA chip requires a different select signal from the KIM-1. The standard signal is the K5 which causes the VIA to be addressed at 1600-160F. Others that can be used are: K1 0600-060F; K2 0A00-0A0F; K3 0E00-0E0F; or, K4 1200-120F. These can not be used if memory has been placed from 0400 to 13FF.


74LS04
2602
2102
JUMPER
ROTARY SWITCHES
74LS138
74LS00
ROM SELECT
RAM SELECT
R/W
340T-5
340T-24
3-5 MFD
.01 MFD
22-25 MFD
RAM
ROM AND SUPPORT
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SCALE: NONE
DATE MAY 26, 1978
APPROVED BY
ROBERT M. TRAPP
DRAWN BY OLLIE HOLT
REVISED JIM WITT
RAM AND POWER
DRAWING NUMBER
MP 1



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EPROMS AND VIA

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